



## STPC Client Motherboard Start-Up

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### 1. Overview.

This document provides detailed information regarding the way to start-up a new STPC Client Motherboard. This document intends to eliminate basic hardware problem which will prevents the STPC Client from start working.

The following "procedure" is a step by step one. Therefore in this document we assume that you have followed this step by step way and that you do not "jump" to a specific item but follow the complete process.

This document is intended to support the following device:

STPC Client

For additional information on the STPC Client specifications, please refer to the STPC Client Databook. Information in this document is subject to change without notification.

**STMicroelectronics values your feedback. Please send it and any recommendations you may have regarding this document to [stpc.support@st.com](mailto:stpc.support@st.com) with the subject line "AN1080".**

### 2. STPC Client Checking.

Four main conditions can prevent an STPC Client Motherboard from working:

- Power Supply
- STPC Configuration
- Clock Circuitry
- Reset Circuitry

#### 2.1 Power Supply.

It is an obvious statement that an defectif or incorrect Power Supply may generate unreliable behavior by the STPC Client. Nevertheless, the STPC has several different Power domains that should be checked when starting-up a new STPC motherboard.

## APPLICATION NOTE

Before powering-up your STPC Client, please verify that the Power Pins are correctly connected according to the following table:

**TABLE 1. STPC Client Power Pins Connections**

Pin Name	Pin Function	Pin Number	Required Voltage
VDD	Logic PS	B14, C9, D6, D11, D16, D21, F4, F23, G1, K23, L4, L23, P2, T4, T23, T26, AA4, AA23, AB23, AC6, AC11, AC16, AC21	3.3V+/-0.3
VDD5	5V/I/O tol.	A16, B12, B9, D18	5V +/- 0.5
VDDE	Logic PS*	AF13, AD19	3.3V+/-0.3
VDD_DAC1/2	DAC PS*	AC7, AF4	3.3V+/-0.3
VDD_GCLK_PLL	GCLK_PLL PS*	WA	3.3V+/-0.3
VDD_DCLK_PLL	DCLK_PLL PS*	AB1	3.3V+/-0.3
VDD_HCLK_PLL	HCLK_PLL PS*	F26	3.3V+/-0.3
VDD_DEVCLK_PLL	DEVCLK_PLL PS*	G24	3.3V+/-0.3

\* PS means Power Supply.

Ground connections are also important for the chip behavior. Please verify that the Ground Pins are correctly connected according to the following table.

**TABLE 2. STPC Client Ground Pins Connections**

Pin Name	Pin Function	Pin Number
VSS	Logic GND	A1, A2, A26, B2, B25, B26
		C3, C24, D4, D9, D14, D19
		D23, H4, J23, L11:16,
		M11:16, N4, N11:16,
		P11:16, P23, R11:16,
		T11:16, V4, W23, AC4,
		AC8, AC13, AC18, AC23,
		AD3, AD24, AE1, AE2,
		AE25, AF1, AF25, AF26
VSS_DAC1/2	DAC GND	AE7, AF7
VSS_PLL	All PLLs GND	E25, E26

## 2.2 STPC Client Configuration

STPC Client has been designed in a way to allow configurations for test purpose that differs from the functional configuration. Assuming that you have checked that the STPC is properly powered (see 2.1), the next step consists in checking that the STPC Client Configuration is correct.

STPC Client is configured at the rising edge of PWERGD (?or SYSRESET).

**TABLE 3. STPC Client Configuration**

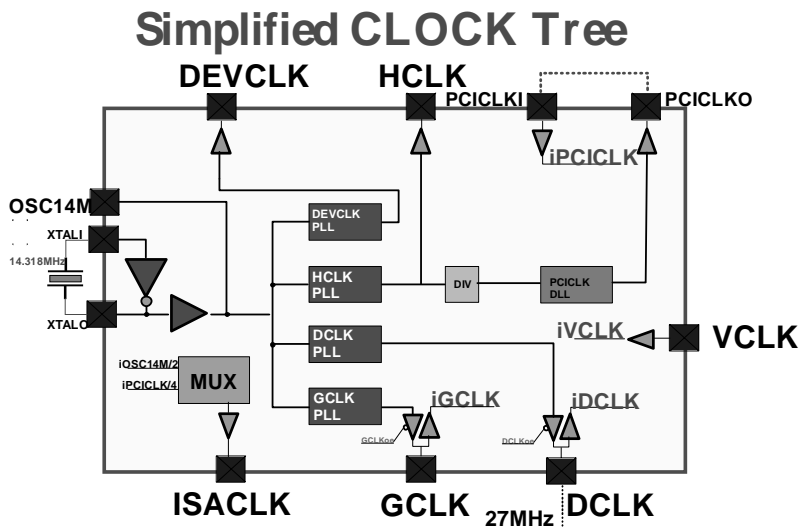
Pin Name	Pin Number	Expected Configuration	Notes (*)
ST0:3	B4, D5, A4, C5	4.7K Pup	STPC as STPC
CLKDELO	C7	4.7K Pdn	For DX2 Mode
CLKDEL1	B5	4.7K Pup	For DX2 Mode
CLKDEL2	A5	4.7K Pdn	For DX2 Mode
MD31	G26	4.7K Pdn	HCLK Skew
MD32	AD22	4.7K Pup	HCLK Skew
MD33	AD23	4.7K Pup	HCLK Skew
MD34	AE26	4.7K Pdn	HCLK Skew
MD35	AD26	4.7K Pup	HCLK Skew
MD16	U24	4.7K Pup	Test Bus Off
MD17	R26	4.7K Pup	PCICLK=HCLK/2
MD19	P26	4.7K Pdn	Int. PLL for GCLK
MD20	N25	4.7K Pup	
MD21	N26	4.7K Pup	
MD22	M25	4.7K Pup	
MD23	M26	4.7K Pup	

MD24:MD26 must have 4.7Pup or 4.7Pdn according to the frequency that has been selected for HCLK.

(\*) Notes are often meaningless for the STPC Client users

## 2.3 Clock Circuitry

STPC Client has a complex Clock Circuitry that allows the generation of all external frequencies from a single 14.318MHz Crystal Oscillator. This simplifies the board design but means also that a default in the clock input can generate a bad behavior of the STPC Client. (See below the STPC Internal Clock Tree).



Assuming that you have checked that the STPC is properly powered (see 2.1) and properly configured (see 2.2), the next step consists in checking the Clock circuitry. For this please check it in the following order:

**TABLE 4. STPC Client Clocks**

Pin Name      Pin Number		Expected Clock Value	Possible cause of problem
XTALO	AE16	14.318MHz	Bad Osc. short on BD*
OSC14M	C6	14.318MHz	Bad conf ST[0..6]
DEV_CLK	F25	24MHz	short on BD*
HCLK	G23	66MHz (dep. Sel)	sh. on BDx*
GCLK2X	AC5	yyMHz	sh. on BD*/bad Conf MDxx
DCLK	AD5	zzMHz	sh. on BD*/bad DCLKDIR
PCI_CLKO	D25	HCLK/2or 3(dep. Sel)	sh. on BD*
PCI_CLKI	F24	PCI_CLKO	Mis with PCI_CLKO

BD means Board.

## 2.5 Reset Circuitry.

Reset of the STPC is used internally to latched configuration strap values on the MD bus. Therefore a bad or missing Reset signal can generate an unexpected behavior of the STPC Client.

Assuming that you have checked that the STPC is properly powered (see 2.1), properly configured (see 2.2) and has the proper clocks, the next step consists in checking the Reset Circuitry. For that please check it in the following order:

**TABLE 5. STPC Client Reset Circuitry**

Pin Name	Pin Number	Expected Behavior	Possible cause of problem
PWERGD	AF3	High (TTL level) when Power is OK. Low (TTL level) when Power is Not OK or reset button is pressed	Sh. on BD/Miss. Connect to PS or reset button
SYSRESET0x	AE4	High when PWERGD is high sh.on BD. Low when PWERGD is low.	

Once the former steps has been checked, the STPC Client by itself should be working fine. Additional problems can come from the board design itself or the SIO that has been selected.

When the STPC is working fine the signal RMRTCCS (P1) is activated after Power On and as long as the ROMBIOS Flash is accessed.

The SIO configuration can also create problems during the boot phase, therefore it is important to refer to the relevant documentation to check that it has been properly configured.

[illegible]

GND	GND	ST6	ST2	CLKDE L2	LOCK#	STOR#	FRAME#	CBE2#	ADB1	AD27	AD24	AD21	AD17	AD14	VDD5	ADB	AD6	AD3	AD0	PCI REQ1#	VCC	DACK _ENC1	DREQ _MUX0	PCI _INT2	GND	
PRQ	GND	ST4	ST0	CLKDE L1	PAR	TRDY#	CBE3#	VDD5	ADB9	AD26	VDD5	AD19	VCC	AD13	AD11	AD7	AD5	AD2	PCI _REQ2#	PCI _GNT1#	DACK _ENC2	DREQ _MUX1	PCI _INT3	GND	GND	
PRQ	SRQ	GND	ST5	ST3	OSC1#	CLKDE L0	DEVSEL #	VCC	CBE1#	ADB0	AD26	AD23	AD22	AD18	AD15	AD12	ADB	AD4	AD1	PCI REQ0#	PCI _GNT0#	DACK _ENC0	GND	IRQ _MUX3	PCI _INT1	
SDACK#	SDRQ	PDACK#	GND	ST1	VCC	SERR#	IRDY#	GND	CBE0#	VCC	ADB8	ADB0	GND	AD16	VCC	AD10	VDD5	GND	PCI _GNT2#	VCC	TC	GND	PCI _INT0	PCI _CLK	IRQ _MUX1	
SLOW#	FIOR#	SOR#	FIOW#	STPC Client TOP VIEW PIN-OUT																		IRQ _MUX0	IRQ _MUX2	VSS _DLL	VSS _DLL	
LA20	LA17	LA19	VCC																			VCC	PCI _CLK	DEV _CLK	VDD_HCLK	
VCC	LA21	L22	LA18																			HCLK	VDD_DE V	MD30	MD81	
SA1	LA23	SA2	GND																			MD62	MD63	MD60	MD29	
SA4	SA3	SA6	SA0																			GND	MD61	MD27	MD28	
SA7	SA5	DD2 _SA10	DD0 _SA8																			VCC	MD69	MD67	MD68	
DD3 _SA11	DD1 _SA9	DD6 _SA14	VCC																			VCC	MD66	MD65	MD66	
DD5 _SA13	DD4 _SA12	DD10 _SA18	DD8 _SA16																			MD25	MD24	MD22	MD23	
DD9 _SA17	DD7 _SA15	DD14 _KBCK#	GND																			MD52	MD54	MD20	MD21	
DD15 _VCC	DD12 _RTCD5	DD11 _SA19																				GND	MD63	MD18	MD19	
SD0	DD13 _SD2	SD4		MD50	MD61	MD48	MD17																			
SD3	SD1	SD6	VCC	STPC Client TOP VIEW PIN-OUT																			VCC	MD49	MD47	VCC
SD7	SD5	SD10	SD8																				MD15	MD16	MD45	MD46
SD11	SD9	SD14	GND																				MD11	MD14	MD44	MD13
SD13	SD12	ALE	VDD_GCLK																				GND	MD12	MD42	MD43
IOCHRDY	SD15	SMEMR#	MEMR#																				MD29	MD10	MD9	MD41
MEMW#	SEHE#	IOR#	VCC																				VCC	MD8	MD7	MD40
VDD_DCLK	SMEMW#	IOWS#	MASTE R#																				VCC	MD6	MD37	MD38
MCS19#	IOW#	AEN	GND	GCLK2X	VCC	VDD_DAC1	GND	COMP	TV_YUV1	VCC	VIDEO_D1	GND	VIDEO_D4	MA2	VCC	MA6	GND	RAS#	CAS#	VCC	MWE#	GND	MD6	MD4	MD5	
IOCHK#	REF#	GND	SYSCLK	DCLK	GREEN	VREF	DDO0	VTV_BT#	TV_YUV3	TV_YUV7	VIDEO_D2	VIDEO_D6	VIDEO_CLK	MA0	MA4	MA8	RAS0#	VCC	CAS#	CAS#	MD32	MD33	GND	MD3	MD35	
GND	GND	GPIOCS#	SYSRST#	ISA_CLK2X	RED	VSS_DAC1	RSET	VSYN	VTV_HSYN	TV_YUV2	TV_YUV5	VIDEO_D0	VIDEO_D3	VIDEO_D7	XTALO	MA3	MA7	MA10	RAS#	CAS0#	CAS#	CAS#	MD1	GND	MD34	
GND	ISAOE#	PWERR_D	VDD_DAC2	DCLK_DIR	BLUE	VSS_DAC2	DDC1	HSYN	TV_YUV0	TV_YUV4	TV_YUV6	VCC	VIDEO_D5	XTALI	MA1	MA5	MA9	MA11	RAS#	CAS#	CAS#	MD0	MD2	GND	GND	

A1/1	A2/2	A3/3	A4/4	A5/5	A6/6	A7/7	A8/8	A9/9	A10/10	A11/11	A12/12	A13/13	A14/14	A15/15	A16/16	A17/17	A18/18	A19/19	A20/20	A21/21	A22/22	A23/23	A24/24	A25/25	A26/26	A27/27	A28/28	A29/29	A30/30																																
B1/2	B2/3	B3/4	B4/5	B5/6	B6/7	B7/8	B8/9	B9/10	B10/11	B11/12	B12/13	B13/14	B14/15	B15/16	B16/17	B17/18	B18/19	B19/20	B20/21	B21/22	B22/23	B23/24	B24/25	B25/26	B26/27	B27/28	B28/29	B29/30	B30/31																																
C1/3	C2/2	C3/5	C4/8	C5/10	C6/15	C7/22	C8/31	C9/43	C10/57	C11/73	C12/91	C13/111	C14/133	C15/157	C16/183	C17/211	C18/241	C19/273	C20/307	C21/343	C22/381	C23/421	C24/463	C25/507	C26/553	C27/601	C28/651	C29/703	C30/757																																
D1/4	D2/30	D3/55	D4/82	D5/108	D6/136	D7/165	D8/195	D9/226	D10/258	D11/291	D12/325	D13/361	D14/398	D15/437	D16/477	D17/518	D18/560	D19/603	D20/647	D21/693	D22/741	D23/791	D24/843	D25/897	D26/953	D27/1011	D28/1071	D29/1133	D30/1197																																
E1/5	E2/31	E3/57	E4/83	<div>STPC Client</div> <div>TOP VIEW</div> <div>BGA-pin/Crad-pin</div> <div>Correspondence</div> <table><tr><td>L1/157</td><td>L12/171</td><td>L13/185</td><td>L14/199</td><td>L15/213</td><td>L16/227</td></tr><tr><td>M1/158</td><td>M12/172</td><td>M13/186</td><td>M14/200</td><td>M15/214</td><td>M16/228</td></tr><tr><td>N1/159</td><td>N12/173</td><td>N13/187</td><td>N14/201</td><td>N15/215</td><td>N16/229</td></tr><tr><td>P1/160</td><td>P12/174</td><td>P13/188</td><td>P14/202</td><td>P15/216</td><td>P16/230</td></tr><tr><td>R1/161</td><td>R12/175</td><td>R13/189</td><td>R14/203</td><td>R15/217</td><td>R16/231</td></tr><tr><td>T1/162</td><td>T12/176</td><td>T13/190</td><td>T14/204</td><td>T15/218</td><td>T16/232</td></tr></table>																		L1/157	L12/171	L13/185	L14/199	L15/213	L16/227	M1/158	M12/172	M13/186	M14/200	M15/214	M16/228	N1/159	N12/173	N13/187	N14/201	N15/215	N16/229	P1/160	P12/174	P13/188	P14/202	P15/216	P16/230	R1/161	R12/175	R13/189	R14/203	R15/217	R16/231	T1/162	T12/176	T13/190	T14/204	T15/218	T16/232	E23/289	E24/315	E25/341	E26/367
L1/157	L12/171	L13/185	L14/199																			L15/213	L16/227																																						
M1/158	M12/172	M13/186	M14/200																			M15/214	M16/228																																						
N1/159	N12/173	N13/187	N14/201																			N15/215	N16/229																																						
P1/160	P12/174	P13/188	P14/202																			P15/216	P16/230																																						
R1/161	R12/175	R13/189	R14/203																			R15/217	R16/231																																						
T1/162	T12/176	T13/190	T14/204																			T15/218	T16/232																																						
F1/6	F2/32	F3/58	F4/84																			F23/290	F24/316	F25/342	F26/368																																				
G1/7	G2/33	G3/59	G4/85																			G23/291	G24/317	G25/343	G26/369																																				
H1/8	H2/34	H3/60	H4/86																			H23/292	H24/318	H25/344	H26/370																																				
J1/9	J2/35	J3/61	J4/87	J23/293	J24/319	J25/345	J26/371																																																						
K1/10	K2/36	K3/62	K4/88	K23/294	K24/320	K25/346	K26/372																																																						
L1/11	L2/37	L3/63	L4/89	L23/295	L24/321	L25/347	L26/373																																																						
M1/12	M2/38	M3/64	M4/90	M23/296	M24/322	M25/348	M26/374																																																						
N1/13	N2/39	N3/65	N4/91	N23/297	N24/323	N25/349	N26/375																																																						
P1/14	P2/40	P3/66	P4/92	P23/298	P24/324	P25/350	P26/376																																																						
R1/15	R2/41	R3/67	R4/93	R23/299	R24/325	R25/351	R26/377																																																						
T1/16	T2/42	T3/68	T4/94	T23/300	T24/326	T25/352	T26/378																																																						
U1/17	U2/43	U3/69	U4/95	U23/301	U24/327	U25/353	U26/379																																																						
V1/18	V2/44	V3/70	V4/96	V23/302	V24/328	V25/354	V26/380																																																						
W1/19	W2/45	W3/71	W4/97	W23/303	W24/329	W25/355	W26/381																																																						
Y1/20	Y2/46	Y3/72	Y4/98	Y23/304	Y24/330	Y25/356	Y26/382																																																						
AA1/21	AA2/47	AA3/73	AA4/99	AA23/305	AA24/331	AA25/357	AA26/383																																																						
AB1/22	AB2/48	AB3/74	AB4/100	AB23/306	AB24/332	AB25/358	AB26/384																																																						
AC1/23	AC2/49	AC3/75	AC4/101	AC5/109	AC6/117	AC7/125	AC8/133	AC9/141	AC10/149	AC11/163	AC12/177	AC13/191	AC14/205	AC15/219	AC16/233	AC17/241	AC18/249	AC19/257	AC20/265	AC21/273	AC22/281	AC23/307	AC24/333	AC25/359	AC26/385																																				
AD1/24	AD2/50	AD3/76	AD4/102	AD5/110	AD6/118	AD7/126	AD8/134	AD9/142	AD10/150	AD11/164	AD12/178	AD13/192	AD14/206	AD15/220	AD16/234	AD17/242	AD18/250	AD19/258	AD20/266	AD21/274	AD22/282	AD23/308	AD24/334	AD25/360	AD26/386																																				
AE1/25	AE2/51	AE3/77	AE4/103	AE5/111	AE6/119	AE7/127	AE8/135	AE9/143	AE10/151	AE11/165	AE12/179	AE13/193	AE14/207	AE15/221	AE16/235	AE17/243	AE18/251	AE19/259	AE20/267	AE21/275	AE22/283	AE23/309	AE24/335	AE25/361	AE26/387																																				
AF1/26	AF2/52	AF3/78	AF4/104	AF5/112	AF6/120	AF7/128	AF8/136	AF9/144	AF10/152	AF11/166	AF12/180	AF13/194	AF14/208	AF15/222	AF16/236	AF17/244	AF18/252	AF19/260	AF20/268	AF21/276	AF22/284	AF23/310	AF24/336	AF25/362	AF26/388																																				

STPC Client  
TOP VIEW  
BGA-pin/Qrcad-pin  
Correspondence

L11/157	L12/171	L13/185	L14/199	L15/213	L16/227
M11/158	M12/172	M13/186	M14/200	M15/214	M16/228
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R11/161	R12/175	R13/189	R14/203	R15/217	R16/231
T11/162	T12/176	T13/190	T14/204	T15/218	T16/232



GND	PJ_INT2	DREQ_MUX0	DACK_NC1	VCC	PJ_REQ1#	AD0	AD3	AD6	AD9	VDD5	AD14	AD17	AD21	AD24	AD27	AD31	CBE2#	FRAME#	STOR#	LOCK#	CLKDE_L2	ST2	ST6	GND	GND
GND	GND	PJ_INT3	DREQ_MUX1	DACK_ENC2	PJ_GNT1#	PJ_REQ2#	AD2	AD5	AD7	AD11	AD13	VCC	AD19	VDD5	AD25	AD29	VDD5	CBE3#	TRDY#	PAR	CLKDE_L1	ST0	ST4	GND	R/RQ
PJ_INT1	IRQ_MUX3	GND	DACK_ENC0	PJ_GNT0#	PJ_REQ0#	AD1	AD4	AD6	AD12	AD15	AD18	AD22	AD23	AD26	AD30	CBE1#	VCC	DEVSEL#	CLKDE_L0	OSC14M	ST3	ST5	GND	S/RQ	PDRQ
IRQ_MUX1	PJ_CLK	PJ_INT0	GND	TC	VCC	PJ_GNT2#	GND	VDD5	AD10	VCC	AD16	GND	AD20	AD28	VCC	CBE0#	GND	IRDY#	SERR#	VCC	ST1	GND	PDACK#	S/RQ	SDACK#
VSS_DLL	VSS_DLL	IRQ_MUX2	IRQ_MUX0																		O	ROW#	S/OR#	P/OR#	S/OW#
VDD_HCLK	DEV_CLK	PJ_CLK1	VCC																			VCC	LA19	LA17	LA20
MD31	MD30	VDD_DE_V	HCLK																			LA18	L22	LA21	VCC
MD29	MD30	MD63	MD62																			GND	SA2	LA23	SA1
MD28	MD27	MD61	GND																			SA0	SA6	SA3	SA4
MD58	MD57	MD59	VCC																			DD0_SA8	DD2_SA10	SA5	SA7
MD56	MD55	MD56	VCC																			VCC	DD6_SA14	DD1_SA9	DD3_SA11
MD23	MD22	MD24	MD25																			DD8_SA16	DD10_SA18	DD4_SA12	DD5_SA13
MD21	MD20	MD54	MD52																			GND	DD14_KBCS#	DD7_SA15	DD9_SA17
MD19	MD18	MD63	GND																			DD11_SA19	DD12_RTCD5	VCC	DD15
MD17	MD48	MD61	MD60																			SD4	SD2	DD13	SD0
VCC	MD47	MD49	VCC																			VCC	SD6	SD1	SD3
MD46	MD45	MD16	MD15																			SD8	SD10	SD5	SD7
MD13	MD44	MD14	MD11																			GND	SD14	SD9	SD11
MD43	MD42	MD12	GND																			VDD_GC_LK_RLL	ALE	SD12	SD13
MD41	MD9	MD10	MD39																			MEMR#	SMEMR#	SD15	IOCHRDY
MD40	MD7	MD8	VCC																			VCC	IOR#	SEHE#	MEMW#
MD38	MD37	MD6	VCC																			MASTE_R#	I/OCS16#	SMEMW#	VDD_GC_LK_RLL
MD5	MD4	MD36	GND	MWE#	VCC	CAS1#	RAS2#	GND	MA6	VCC	MA2	VIDEO_D4	GND	VIDEO_D1	VCC	TV_YUV1	COMP	GND	VDD_DAC1	VCC	GLK2X	GND	AEN	IOW#	MCS16#
MD35	MD8	GND	MD33	MD32	CAS#	CAS3#	VCC	RAS0#	MA8	MA4	MA0	VIDEO_D6	VIDEO_D6	VIDEO_D2	TV_YUV7	TV_YUV3	VTV_BT#	DD0	VREF	GREEN	DCLK	SYCLK	GND	REF#	IOCH#
MD34	GND	MD1	CAS#	CAS#	CAS#	RAS1#	MA10	MA7	MA3	XTALO	VIDEO_D7	VIDEO_D3	VIDEO_D0	TV_YUV5	TV_YUV2	VTV_HSYNC	VSYSNC	RSET	VSS_DAC1	RED	ISA_CLK2X	SYSRST#	GPIOCS#	GND	GND
GND	GND	MD2	MD0	CAS#	CAS#	RAS3#	MA11	MA9	MA5	MA1	XTAL1	VIDEO_D5	VCC	TV_YUV6	TV_YUV4	TV_YUV0	HSYNC	DDC1	VSS_DAC2	BLUE	DCLK_DIR	VDD_DAC2	PWERRD	ISAOE#	GND

STPC Client  
BOTTOM VIEW  
PIN-OUT

GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND

	GND		DRAM
	VCC		VIDEO
	VDD		VGA
	PJ		ISAVIDE

### 4. Technical Support

STMicroelectronics is on the Internet with a worldwide web (WWW) site on which product presentation, technical literature as well as product support information can be found.

A dedicated STPC section is available providing up to date hardware documentation and software tools.

The Web and e-mail addresses are:

**WWW : *<http://www.st.com/stpc>***

**e-mail : *[stpc.support@st.com](mailto:stpc.support@st.com)***

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5. Update History for Application Note AN 1080

The following changes have been made to the Application Note AN 1080 from Revision 1.0 to Release 1.1.

Page	Section	Change	Text
3	2.2	Replaced	Cell MD31 Expected Configuration from “ <del>4.7KPup</del> ” to “4.7KPdn”
3	2.2	Replaced	Cell MD32 Expected Configuration from “ <del>4.7KPdn</del> ” to “4.7KPup”
3	2.2	Replaced	Cell MD34 Expected Configuration from “ <del>4.7KPup</del> ” to “4.7KPdn”
3	2.2	Replaced	Cell MD35 Expected Configuration from “ <del>4.7KPdn</del> ” to “4.7KPup”
3	2.2	Replaced	Cell MD19 Expected Configuration from “ <del>4.7KPdn</del> ” to “4.7KPup”

